AMENDMENTS

In The Claims:

1. (currently amended) An extended bus structure, for coupling with a control chip set, the control chip set also coupled with a central processing unit, a system memory, and a bus, the extended bus structure comprising:

a first accelerated graphics port bus, for coupling with the control chip set;

a first extended bus for expanding the first accelerated graphics port bus; and

a first bridge coupled to the first accelerated graphics port bus and the first extended bus for converting mutually and compatibly signal and data between the first accelerated graphics port bus and the first extended bus, wherein the first bridge is not directly coupled to the control chip set.

2. (original) The extended bus structure of claim 1, wherein the first bridge further comprises:

a main accelerated graphics port controller coupled to the first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof;

a first extended bus controller coupled to the first extended bus for compatibly receiving and transmitting data and signal thereof; and

a flow controller coupled to the main accelerated graphics port controller and the first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller and the first extended bus controller.

3. (original) The extended bus structure of claim 1, further comprising:

a second accelerated graphics port bus coupled to the first bridge to expand the first accelerated graphics port bus, wherein data and signal of the first and second accelerated graphics port buses are mutually and compatibly converted by the first bridge.

4. (original) The extended bus structure of claim 3, wherein the first bridge further comprises:

a main accelerated graphics port controller coupled to the first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof;

a first extended bus controller coupled to the first extended bus for compatibly receiving and transmitting data and signal thereof;

an extended accelerated graphics port controller coupled to the second accelerated graphics port bus for compatibly receiving and transmitting data and signal of the second accelerated graphics port bus; and

a flow controller coupled to the main accelerated graphics port controller, the extended accelerated graphics port controller, and the first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller, the extended accelerated graphics port controller, and the first extended bus controller.

5. (original) The extended bus structure of claim 3, further comprising:

a second extended bus to expand the second accelerated graphics port bus; and

a second bridge coupled to the second accelerated graphics port bus and the second extended bus for converting mutually and compatibly data and signal of the second accelerated graphics port bus and the second extended bus.

6. (original) The extended bus structure of claim 3, further comprising:

a second accelerated graphics port bus coupled to the first bridge for expanding the first accelerated graphics port bus, wherein the first bridge compatibly converts data and signal of the first accelerated graphics port bus and the second extended bus.

7. (original) The extended bus structure of claim 6, wherein first bridge comprises:

a main accelerated graphics port controller coupled to the first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof;

a first extended bus controller coupled to the first extended bus for compatibly receiving

and transmitting data and signal thereof;

a second extended bus controller coupled to the second extended bus for compatibly receiving and transmitting data and signal of the second extended bus; and

a flow controller coupled to the main accelerated graphics port controller and the first and second extended bus controllers for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller, the first and second extended bus controllers.

8. (original) The extended bus structure of claim 1, further comprising a control chip set coupled to the first accelerated graphics port bus.

9. (original) The extended bus structure of claim 1, further comprising a peripheral coupled to the first extended bus.

10. (currently amended) A bridge, comprising:

a main accelerated graphics port controller coupled to [[~~the~~]]a first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof, wherein the first accelerated graphic port bus is for coupling with a control chip set, and the control chip set is also coupled with a central processing unit, a system memory, and a bus, wherein the main accelerated graphics port controller is coupled to the first accelerated graphics port bus but not directly coupled to the control chip set;

a first extended bus controller coupled to the first extended bus for compatibly receiving and transmitting data and signal thereof; and

a flow controller coupled to the main accelerated graphics port controller and the first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller and the first extended bus controller.

11. (original) The bridge of claim 10,further comprising:

an extended accelerated graphics port controller coupled to the second accelerated graphics port bus and the flow controller for compatibly receiving and transmitting data and

signal of the second accelerated graphics port bus, wherein the flow controller arbitrates and controls flow direction of data and signal of the main accelerated graphics port controller, the first extended bus controller, and the extended accelerated graphics port controller.

12. (original) The bridge of claim 10, further comprising:

a second extended bus controller coupled to the second extended bus and the flow controller for compatibly receiving and transmitting data and signal of the second extended bus, wherein the flow controller arbitrates and controls flow direction of data and signal of the main accelerated graphics port controller, the first extended bus controller, and the second extended bus controller.

13. (currently amended) A method for extending a bus to expand a first accelerated graphics port bus, comprising:

providing a first extended bus; and

compatibly and mutually converting data and signal of the first accelerated graphics port bus and the first extended bus, wherein the first accelerated graphic port bus is for coupling with a control chip set, and the control chip set is also coupled with a central processing unit, a system memory, and a bus, wherein the first extended bus is not directly coupled with the control chip set.

14. (original) The method of claim 13, further comprising:

providing a second accelerated graphics port bus; and

compatibly and mutually converting data and signal of the first accelerated graphics port bus and the second accelerated graphics port bus.

15. (original) The method of claim 13, further comprising:

providing a second extended bus; and

compatibly and mutually converting data and signal of the first accelerated graphics port bus and the second extended bus.